IN THE CLAIMS

Please amend the claims as follows:

1. (Currently amended) An integrated circuit comprising:

a despreading unit operative to despread input samples and provide despread symbols for a first code channel with a first spreading factor;

a channel compensation unit operative to multiply the despread symbols with channel estimates and provide demodulated symbols for the first code channel; and

a symbol combiner operative to combine groups of demodulated symbols for at least two symbol periods of the first code channel to obtain recovered data symbols for a second code channel with a second spreading factor that is an integer multiple of the first spreading factor.

2. (Original) The integrated circuit of claim 1, wherein the second spreading factor is two times the first spreading factor.

3. (Original) The integrated circuit of claim 1, wherein the symbol combiner is operative to combine groups of demodulated symbols to obtain recovered data symbols for a third code channel with the second spreading factor.

4. (Original) The integrated circuit of claim 1, wherein the channel compensation unit is operative to multiply each of the despread symbols with a channel estimate for one transmitter antenna to obtain one demodulated symbol for the despread symbol.

5. (Original) The integrated circuit of claim 4, wherein the symbol combiner is operative to combine groups of two demodulated symbols for two symbol periods of the first code channel to obtain the recovered data symbols for the second code channel.

6. (Original) The integrated circuit of claim 1, wherein the channel compensation unit is operative to multiply each of the despread symbols with channel

estimates for two transmitter antennas to obtain two demodulated symbols for the despread symbol.

7. (Original) The integrated circuit of claim 6, wherein the symbol combiner is operative to combine groups of four demodulated symbols for four symbol periods of the first code channel to obtain the recovered data symbols for the second code channel.

8. (Original) The integrated circuit of claim 1, wherein the symbol combiner is operative to combine groups of demodulated symbols based on space time transmit diversity (STTD).

9. (Currently amended) The integrated circuit of claim 1, wherein the second code channel is a high-speed physical downlink shared channel (HS-PDSCH) in Wideband Code Division Multiple Access (W-CDMA) Release 5 or later.

10. (Currently amended) The integrated circuit of claim 1, wherein the second code channel is a packet data channel (PDCH) in IS-2000 Release C or later.

11. (Currently amended) A device in a Code Division Multiple Access (CDMA) communication system, comprising:

a despreading unit operative to despread input samples and provide despread symbols for a first code channel with a first spreading factor;

a channel compensation unit operative to multiply the despread symbols with channel estimates and provide demodulated symbols for the first code channel; and

a symbol combiner operative to combine groups of demodulated symbols for at least two symbol periods of the first code channel to obtain recovered data symbols for a second code channel with a second spreading factor that is an integer multiple of the first spreading factor.

12. (Original) The device of claim 11, wherein the channel compensation unit is operative to multiply each despread symbol with channel estimates for two transmitter antennas to obtain two demodulated symbols for the despread symbol, and wherein the

symbol combiner is operative to combine groups of four demodulated symbols for four symbol periods of the first code channel to obtain the recovered data symbols for the second code channel.

13. (Currently amended) An apparatus in a Code Division Multiple Access (CDMA) communication system, comprising:

means for despreading input samples to obtain despread symbols for a first code channel with a first spreading factor;

means for multiplying the despread symbols with channel estimates to obtain demodulated symbols for the first code channel; and

means for combining groups of demodulated symbols for at least two symbol periods of the first code channel to obtain recovered data symbols for a second code channel with a second spreading factor that is an integer multiple of the first spreading factor.

14. (Currently amended) A processor readable media for storing instructions operable in a wireless device to:

despread input samples to obtain despread symbols for a first code channel with a first spreading factor;

multiply the despread symbols with channel estimates to obtain demodulated symbols for the first code channel; and

combine groups of demodulated symbols for at least two symbol periods of the first code channel to obtain recovered data symbols for a second code channel with a second spreading factor that is an integer multiple of the first spreading factor.

15. (Currently amended) A method of performing data demodulation in a Code Division Multiple Access (CDMA) communication system, comprising:

despreading input samples to obtain despread symbols for a first code channel with a first spreading factor;

multiplying the despread symbols with channel estimates to obtain demodulated symbols for the first code channel; and

combining groups of demodulated symbols for at least two symbol periods of the first code channel to obtain recovered data symbols for a second code channel with a second spreading factor that is an integer multiple of the first spreading factor.

16. (Currently amended) An integrated circuit comprising:

a despreading unit operative to despread input samples and provide despread symbols for a plurality of first code channels with a first spreading factor;

a channel compensation unit operative to multiply the despread symbols for each of the plurality of first code channels with channel estimates and provide demodulated symbols for the first code channel; and

a symbol combiner operative to combine groups of demodulated symbols for at least two symbol periods for each of the plurality of first code channels to obtain recovered data symbols for a set of second code channels with a second spreading factor and corresponding to the first code channel, the second spreading factor being an integer multiple of the first spreading factor.

17. (Original) The integrated circuit of claim 16, wherein the second spreading factor is two times the first spreading factor.

18. (Original) The integrated circuit of claim 17, wherein the symbol combiner is operative to combine groups of four demodulated symbols for four symbol periods of the first code channels based on space time transmit diversity (STTD) to obtain the recovered data symbols.

19. (Original) The integrated circuit of claim 16, wherein the despread symbols for the plurality of first code channels are processed by the channel compensation unit and the symbol combiner in a time division multiplexed (TDM) manner, one first code channel at a time.

20. (Original) The integrated circuit of claim 16, wherein the channel compensation unit and symbol combiner are operated in a pipelined manner.

21. (Original) The integrated circuit of claim 16, further comprising:

a channel selector operative to receive the despread symbols for the plurality of first code channels and provide a despread symbol for one first code channel at a time to the channel compensation unit.

22. (Original) The integrated circuit of claim 21, wherein the channel compensation unit is operative to multiply despread symbols from the channel selector with the channel estimates to obtain the demodulated symbols, and wherein the symbol combiner is operative to combine the demodulated symbols from the channel compensation unit with accumulated symbols to obtain combined symbols, the accumulated symbols being indicative of partial combining results for the recovered data symbols and the combined symbols being indicative of updated combining results for the recovered data symbols.

23. (Original) The integrated circuit of claim 22, further comprising:

a symbol buffer operative to provide the accumulated symbols and store the combined symbols.

24. (Original) The integrated circuit of claim 23, wherein the symbol buffer includes

a first memory bank operative to store combined symbols for a first plurality of second code channels, and

a second memory bank operative to store combined symbols for a second plurality of second code channels.

25. (Original) The integrated circuit of claim 24, wherein the first and second memory banks are alternately accessed.

26. (Currently amended) An apparatus in a Code Division Multiple Access (CDMA) communication system, comprising:

means for despreading input samples to obtain despread symbols for a plurality of first code channels with a first spreading factor;

means for multiplying the despread symbols for each of the plurality of first code channels with channel estimates to obtain demodulated symbols for the first code channel; and

means for combining groups of demodulated symbols for at least two symbol periods for each of the plurality of first code channels to obtain recovered data symbols for a set of second code channels with a second spreading factor and corresponding to the first code channel, the second spreading factor being an integer multiple of the first spreading factor.